the Heath SM-104A—world's most remarkable counter value

Make the cost comparison yourself. No other counter available functions to 80 MHz at this low cost. The SM-104A is in a class by itself... for capability... for design... for reliability... for price.

80 MHz capabiilty at a 15 MHz price. The SM-104A delivers accurate frequency measurement from 10 Hz to over 80 MHz... and does it directly without prescaling.

8-digit capability. To read an unknown frequency less than 100 kHz, place the kHz/MHz time base switch in the kHz position and read direct, down to the last Hz. When the frequency is greater than 100 kHz, the overrange indicator will flash... change the time base switch to the MHz position and read the frequency to the last kHz. In just seconds you can make measurements to more than 80 MHz, with resolution of ±1 Hz ± clock accuracy. Fixed decimal point location eliminates interpolation and figuring.

High sensitivity. The SM-104A requires no more than 100 mV to trigger up to 50 MHz... counts to 80 MHz with only 250 mV RMS input. The FET input completely eliminates input attenuators. See the curve below for information on maximum input voltage versus frequency.

Input impedance of 1 megohm shunted by less than 15 pF provides minimum circuit loading.

"State-of-the-art" design. Twenty-seven integrated circuits, five thick-film resistor packs and nine transistors combine to deliver capability, accuracy and long term dependability unavailable in any competitive counter at any price.

Superspeed Schottky TTL. The SM-104A marks the first commercial use of the new Texas Instruments 74S Series superspeed Schottky TTL integrated circuits... accounting for the high speed and significant cost-reduction found in the SM-104A.

Light-Emitting-Diode readout. Light-emitting diodes — the first really new idea in readout devices since cold-cathode display tubes — are used for all five digits and overrange indication in the SM-104A. The benefits of choosing LEDs over the more conventional cold-cathode display are numerous. The once-standard 170 volt power supply is eliminated completely, reducing cost, instrument complexity, and space. The problems inherent in cold-cathode tubes themselves — limited life and shock susceptibility — do not exist in the LED device. The average half-life of an LED is more than 100 years of typical use. And LEDs are sealed, solid-state devices... there are no fragile filaments to break. The flat, single-plane LED readout offers no chance for parallax and reading error, and is noticeably brighter than other types of displays.

Extremely stable time base. Many other counters with less range and higher price use the incoming line frequency as a standard. With the SM-104A, we went all the way. All gating and timing circuits in the SM-104A are controlled by an extremely precise and stable 1 MHz temperature compensated crystal oscillator (TCXO). Aging rate is 1 part in 10^6/year. Frequency change with temperature is 1 part in 10^6 from 0 to 40 degrees C.

A sophisticated, high-reliability design. The SM-104A exemplifies the modern, state-of-the-art approach to laboratory quality instrumentation: a rugged aluminum chassis and case... double-side, plated-through computer-grade G-10 glass-epoxy circuit board... 5-digit TTL-compatible BCD output... print-command output... handy gimbal mounting bracket that permits use on a bench or mounting under a shelf... simple two-switch operation... switch-selected 120 or 240 VAC operation.

Rigidly quality controlled. All SM-104A components are inspected to rigid standards before they are placed in stock. Assembled counters are 100% inspected for all specification standards. Then *all* SM-104A's are "burned-in" at 40 degrees C to assure absolute performance and reliability. Counters which fail this test are not just repaired, inspected and packaged, but run through the burn-in process again. Quality... in components, assembly and performance... is precisely controlled throughout the entire cycle.

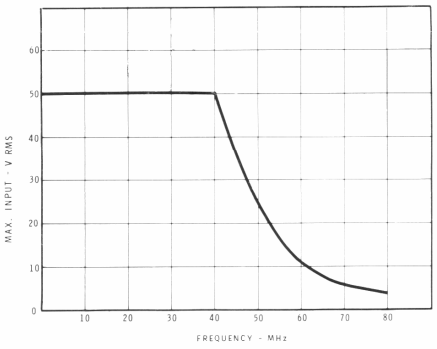
Compare the SM-104A. It delivers more honest capability and value than any counter on the market, at any price. Quantity discounts available... write for details.

Assembled SM-104A, 6 lbs. **$500.00**

Assembled PKW-101 probe increases input impedance to 10 megohms and maximum input voltage to 500 V. Attenuation: x10. 2 lbs. . . **$19.95**

SPECIFICATIONS

Frequency Range: 10 Hz to over 80 MHz. **Sensitivity (after 5 minutes warmup):** 100 mV RMS, to 50 MHz; 250 mV RMS, 50 MHz to 80 MHz. **Input Impedance:** 1 megohm shunted by less than 15 pf. **Maximum Input Voltage:** 50 V RMS (max. DC input is ±50 V; max. AC input is 50 V to 40 MHz — see curve). **Time Base:** 1 MHz, temperature compensated crystal oscillator. **Aging rate:** 1 part in 10^6 per year. **Frequency change with temperature:** 1 part in 10^4, 0 to 40 degrees C. **Readout:** Five 7-segment light-emitting-diode displays, plus one light-emitting-diode for overrange indication. **BCD Output.** Rear panel connector for five digits of BCD (TTL-compatible), Overrange, Print Command (50 usec typical pulse width) and Ground. **Power Requirements:** 120 V, 50/60 Hz, 20 watts. May be changed to 240 V with internal switch and change of fuse. **Dimensions:** 9⅛" D x 6¾" W x 2¼" H. **Net Weight:** 3½ lbs.



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Benton Harbor, Michigan 49022

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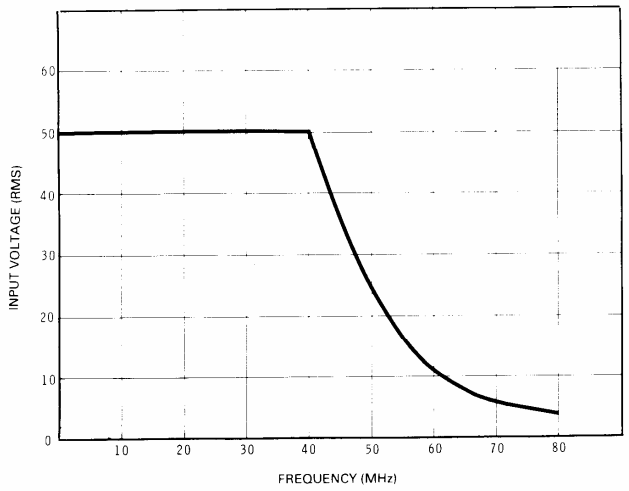


Figure 2-1 — INPUT PROTECTION DERATING CURVE

SECTION 2

SPECIFICATIONS

Frequency Range	10 Hz to over 80 MHz.
Sensitivity (after 5 minute warmup)	100 mV rms, to 50 MHz. 250 mV rms, 50 MHz to 80 MHz.
Input Impedance	1 MΩ, shunted by less than 15 pF.
Maximum Input Voltage	See Derating Curve, Figure 2-1. (Maximum dc input is 50 volts).
Time Base (After 1-hour warm-up)	(SM-104A) 1 MHz. 1 ppm maximum change between 0°C and 40°C ambient temperature. 0.25 sec stability $\pm 1 \times 10^{-9}$. 1-year stability, ± 1 ppm. (SM-105A) 1 MHz ± 2 Hz. ± 10 ppm, 0°C to 40°C ambient, referenced to 25°C.
Readout	Five 7-segment light-emitting diode displays, plus one light-emitting diode for overrange indication.
BCD Output (SM-104A only)	Rear panel connector for BCD, Overrange, Print Command, (50μsec Typical), and Ground.
Power Requirements	105-125V, 50/60 Hz, 20 watts. (210-250V, by changing internal switch and fuse.)
Dimensions	9-1/16" deep, 6-3/4" wide, 2-1/4" high.
Net Weight	3-1/2 pounds.

SECTION 3

OPERATION

The Heath Solid-State Counter has two operational controls: the power On/Off switch and the kHz/MHz time base switch. The time base switch selects a 1 millisecond time base in the MHz position, or 1 second in the kHz position.

To measure an unknown frequency, turn the power switch on and place the time base switch in the kHz position. Allow the counter to reset to zero, then apply the unknown frequency to the input. If the overrange light is not flashing, the unknown frequency is less than 100 kHz and the display is a direct readout of the true frequency in kHz. Digits to the right of the decimal point represents Hz.

If the overrange light is flashing, the unknown frequency is greater than 100 kHz. Change the time base switch to the MHz position and the most significant digit of the unknown frequency will be displayed. In this case, digits to the left of the decimal point will indicate MHz, and digits to the right will indicate kHz.

When counting frequencies greater than 100 kHz with the time base switch in the MHz position, the resolution will be ±1kHz. This resolution can be increased to ±1 Hz by placing the switch in the kHz position. Then frequencies to over 80 MHz can be counted with accuracy of ±1 Hz, ± time base accuracy.

CAUTION: Input protection is provided as shown in the Derating Curve of Figure 2-1. Damage to the instrument can result if excessive voltage is applied to the input.

INPUT CABLES AND PROBES

The input characteristics of the SM-104A and SM-105A Counters are specified on the Derating Curve in Figure 2-1, and in the Specifications on Page 2-1. Any standard 10-megohm, ÷10 oscilloscope probe (such as the Heath PKW-101) will work with this unit when used within the ratings of both the probe and the counter. The input of the counter is ac coupled and there is no dc ÷10, so the input is still limited to the 50-volt dc maximum.

Any cable will work with this counter. However, if coaxial or other transmission line is used, it should be terminated in its characteristic impedance. This will eliminate serious reflections along the line which could damage the equipment under test. The input impedance will then be the characteristic impedance of the transmission line.

The 5-way binding post to BNC adapter, supplied with this counter, can be used to connect the terminating resistor and cable leads to the BNC input. The adapter is also a convenient means of connecting test leads with banana plugs or phone tips, or plain wires.

240 VOLT OPERATION

This instrument is shipped ready for operation from a 105-125 volt power source. If 210-250 volt operation is desired, remove the gimbal bracket and cabinet shell, then place the 120/240 switch in the 240 position. Replace the 1/4 ampere fuse with a 1/8 ampere 240 volt fuse.

NOTE: Electrical regulations in some areas demand a special line cord and/or plug for 240 volt power lines. Replace if required.

This completes the changes necessary for 240 volt operation. Replace the cabinet shell and gimbal bracket on the instrument.

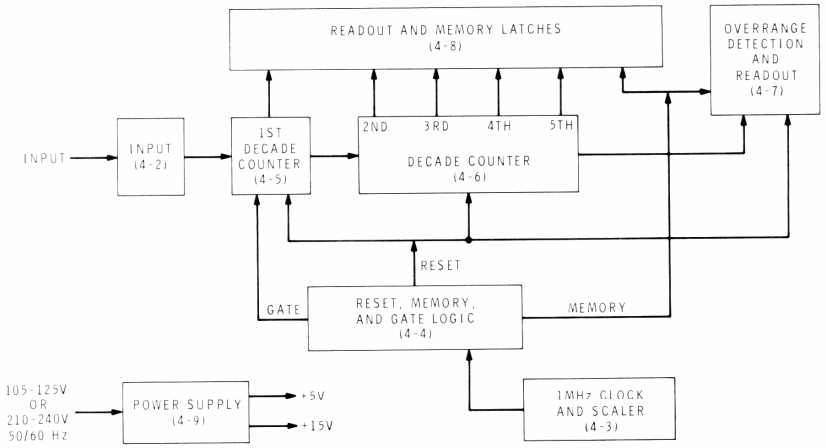
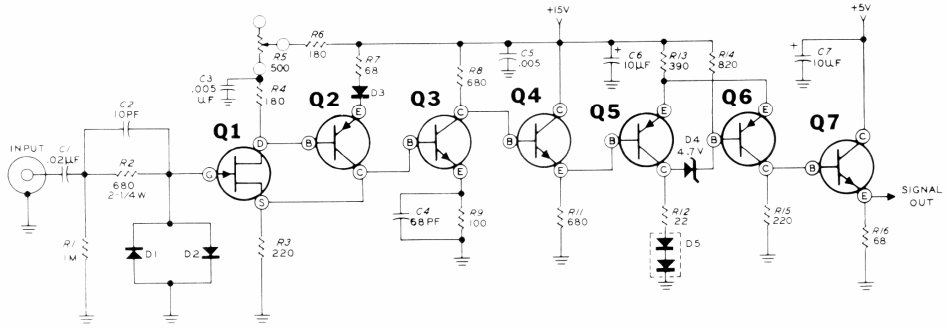


Figure 4-1 — BLOCK DIAGRAM OF SOLID-STATE COUNTER



Note: To adjust for best input sensitivity, connect scope to Q7 emitter (signal out, R16). With low-level sinewave input, adjust R5 (ten turn pot) for symmetric waveform.

Figure 4-2 — INPUT AMPLIFIER AND SCHMITT TRIGGER

SECTION 4

CIRCUIT DESCRIPTION

4-1 GENERAL

The Heath Solid-State Counter consists of an input section, a 1 MHz clock and scaler, a gating circuit, decade counters, overrange detector, readout, and a power supply. The Block Diagram in Figure 4-1 shows the interrelation of these circuits as discussed in the following paragraphs.

The 1 MHz clock and scaler produces an exact time base of 1 second or 1 millisecond that controls all of the gating and timing circuits and determines the overall accuracy of the instrument. The output of the clock and scaler circuit is applied to the reset, gate, and memory circuits which reset the counters, gate the first decade counter for a precise period, and hold the readout display until gated for another count period.

A signal applied to the input circuit is amplified, shaped, and then applied to the first decade counter. When this counter is gated, the pulses from the input and shaper circuit are counted in 1-2-4-8 BCD (binary-coded-decimal) logic, with each tenth pulse passing to the next decade counter. The BCD logic signals from each decade counter pass through memory latches to decoder-drivers that translate the BCD signals into 7-line logic codes which light appropriate segments in the light-emitting diode display. The tenth pulse from the fifth decade counter triggers the overrange detector and readout circuit to cause overrange indication.

Power requirements for the circuits in the counter are provided by the regulated +5 volt and +15 volt power supplies.

Each of the individual circuits will be described separately in the following text. While reading the descriptions, refer to the Block Diagram, the overall Schematic Diagram (fold-out from Page 7-3), and to the Schematics included with each section being described.

4-2 INPUT AMPLIFIER AND SCHMITT TRIGGER

The input circuit consists of a network of capacitors, resistors, and diodes that function as follows: 1) C1 removes any dc component from the input signal, 2) C2 prevents attenuation of high frequency signals, and 3) R2, D1, D2 prevents overload of the input transistors.

Input transistors Q1 and Q2 are direct-coupled with 100% negative feedback to provide wide bandwidth, high input impedance, and approximately unity gain. Transistor Q3 is an amplifier with emitter compensation, isolated from the succeeding Schmitt trigger by emitter-follower Q4.

Schmitt trigger transistors Q5 and Q6 are emitter-coupled for current-mode operation to produce the fast switching times required for the first decade counter. Operating current for the trigger is set by resistor R13, while R14 biases zener diode D4 in its zener region.

Emitter-follower Q7 prevents the TTL logic in the counter circuit from loading the Schmitt trigger.

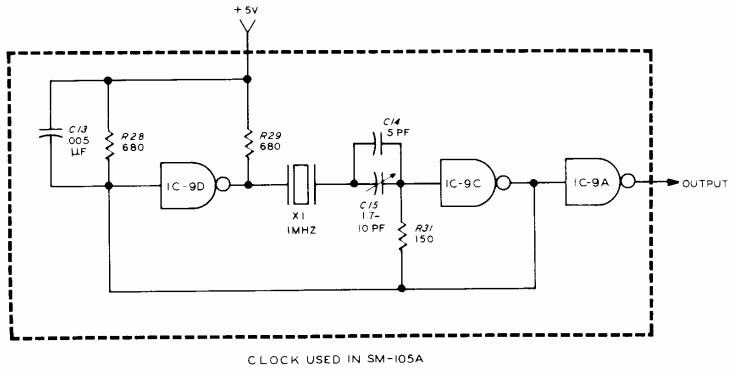


Figure 4-3 — 1 MHz CLOCK AND SCALER

4-3 1 MHz CLOCK AND SCALER

A packaged, temperature-compensated, 1 MHz crystal oscillator is used in the SM-104A. Internal circuitry of this sealed unit will not be discussed in this Circuit Description.

The SM-105A uses a 1 MHz crystal and gates A, C, and D of IC-9 to form a TTL - compatable clock. Capacitors C14 and C15 provide the proper capacitive load for the crystal, with C15 variable for precise calibration of the oscillator. Resistors R28, 29, and 31 bias gates C and D in their linear region for efficient starting.

The scaler consists of six decade dividers connected for a 1-2-4-8 BCD output. Switch S2 selects the D output from the third or sixth divider and either the A output of the fourth divider or the Q output of IC-15A; thereby providing the 1 millisecond (MHz) or 1 second (kHz) time bases for the gating, reset, and memory circuits. The A output of IC-21 provides the memory pulse, and the C output of IC-20 connects to gate IC-9B in the overrange circuit, which will be discussed later.

4-4 GATING, RESET, AND MEMORY

The gating reset and memory circuit controls the time that the following events occur; 1) The unknown input signal is gated into the counting circuits. 2) The accumulated information is passed from the counters to the readout circuits. 3) The counters are reset for a new cycle of counting. The function of this circuit will be discussed with the time base switch first in the MHz position, and later be related to the kHz position. Figure 4-4 shows the circuit and the pulse relationships.

With the time base switch in the MHz position, the "gate open" signal has a 1-millisecond pulse width and is obtained from the A-bit output (pin 12) of IC-19 in the scaler. The unknown input signal enters the counters during the millisecond that the logic 1 of the gating signal is felt on the J and K inputs of the first flip-flop of the first decade divider (pins 2 and 3 of IC-24A).

The reset pulse is derived by combining the inverted gate signal with the D output (pin 11) of IC-18 in NAND gate IC-22B. Therefore, a logic 0 resets the first DCU and the overrange flip-flop whenever the gate is closed (logic 0) and the D output of IC-18 is at a logic 1. This reset pulse is inverted by IC-22D, supplying the logic 1 reset required by the 2nd, 3rd, 4th, and 5th DCU's. These reset pulses occur every 2 milliseconds, immediately prior to the gate opening.

The memory signal is derived by combining the reset pulse (pin 12 of IC-22B) with the inverted gate pulse in nand gate IC-22A, and then inverting the resulant pulse in IC-23A.

The output of IC-23A is combined in NAND gate IC-23C with the differentiated A-bit output of IC-21 in the scaler. Therefore, a memory pulse can occur only when the gate is closed (logic 0), the reset pulse is not present, and the A-bit output of IC-21 is making the transition from a logic 0 to a logic 1.

Although the gate-reset cycle occurs every 2 milliseconds, the differentiated A output of IC-21 permits the memory pulse to occur only every 200M seconds, so 100 count-reset cycles occur for every memory update.

With the time base switch in the kHz position, the gate open time is 1 sec and is obtained from the Q output (pin 12) of IC-15A in the scaler.

The reset pulse is derived in the same manner as with the time base switch in the MHz position, except the basic signals are obtained from the D-bit output (pin 12) of IC-21 and the Q output of IC-15A.

The memory pulse is also derived in the same manner as when the time base switch is in the MHz position except now the gate reset cycle occurs every 2 seconds, while the memory occurs every 0.2 seconds unless inhibited by the presence of either a reset pulse or a gate-open pulse. Therefore, there will be four memory pulses for every gate reset cycle. These extra pulses do not affect the readout since neither gate-open nor reset can occur during these four memory pulses.

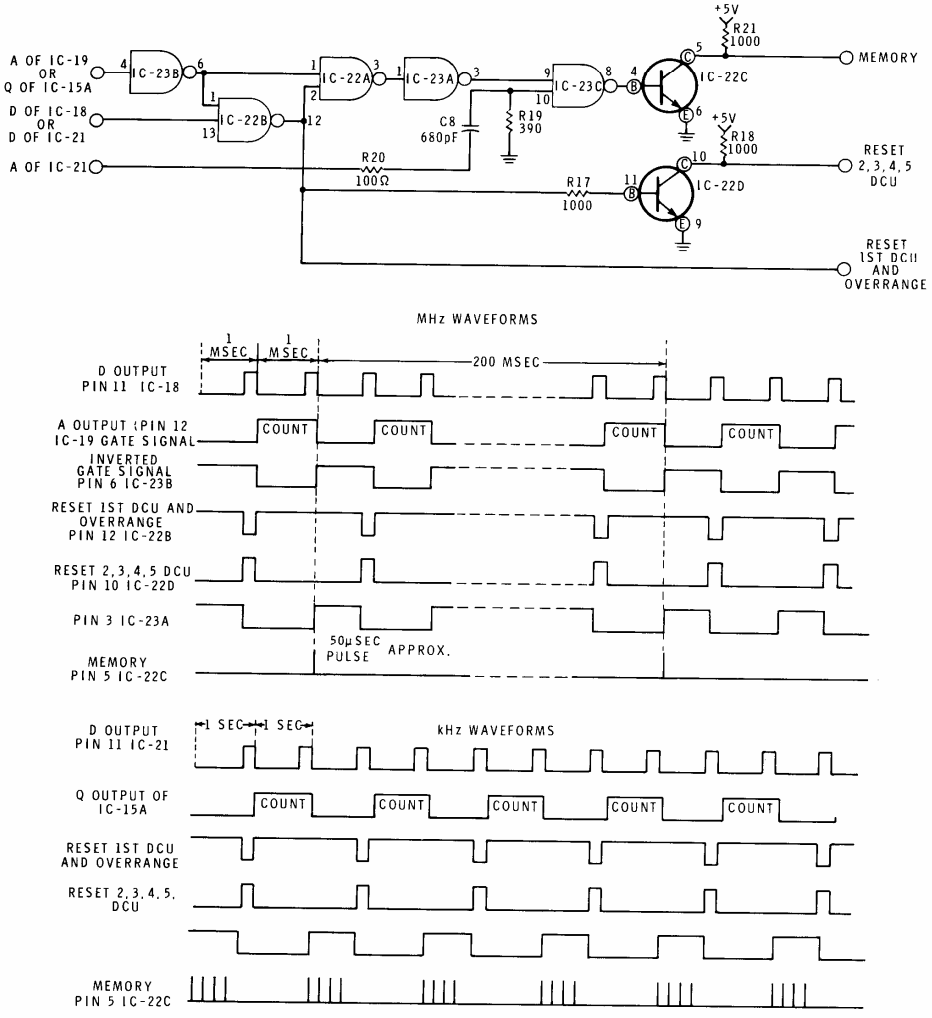
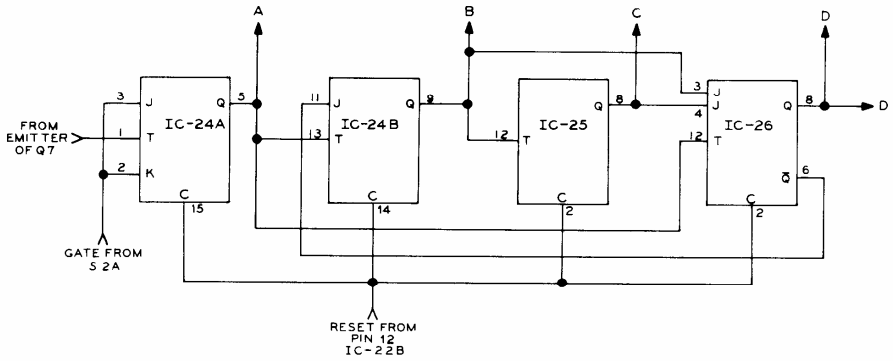
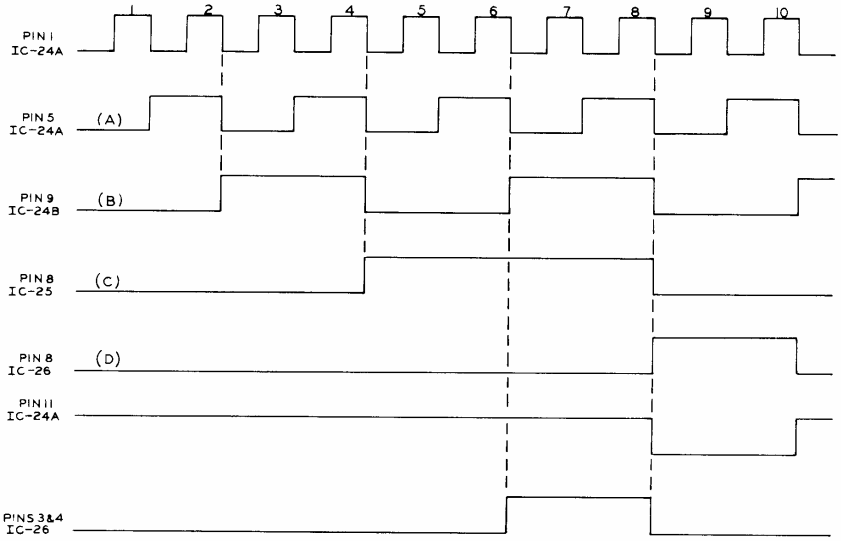


Figure 4-4 — PULSE RELATIONSHIPS OF THE GATE, MEMORY, AND RESET CIRCUIT





COUNT	A	B	C	D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

FIRST DECADE COUNTER

Figure 4-5 — FIRST DECADE COUNTER

4-5 FIRST DECADE COUNTER

The circuit is connected as an asynchronous 1-2-4-8 Binary Coded Decimal (BCD) counter. Flip-flop IC-24A is toggled by the signal from the input amplifier and Schmitt trigger. The flip-flops in the first decade counter are triggered by negative-going pulses. Since IC-24A is toggled on every input pulse when both the J and K inputs are logic 1, the Q output (A) is a logic 1 on the first, third, fifth, seventh, and ninth counts. These pulses are applied to the toggle input of IC-24B. However, due to the feedback loop from Q of IC-26 to the J input of IC-24B, IC-24B is inhibited on the tenth count. As a result, the Q output (B) of IC-24B is a logic 1 for the second, third, sixth, and seventh counts. IC-25 is toggled by the Q output of IC-24B on the fourth and eighth counts. Consequently, the Q output (C) of IC-25 is a logic 1 for the fourth, fifth, sixth, and seventh counts.

Two feed forward loops are incorporated around IC-26, which is toggled by the Q output of IC-24A, to inhibit its toggling on any pulse except the eighth and the tenth count. This is done by connecting the Q outputs of IC-24B and IC-25 to the J inputs of IC-26. As a result, IC-26 will toggle only when both the Q outputs from IC-24B and IC-25 are at logic 1. This results in the Q output (D) of IC-26 being at logic 1 for the eighth and ninth counts only. On the tenth count, IC-24A toggles to a logic 0 at its Q output since its J input is a logic 0. IC-25 will stay at logic 0 since its input was not toggled, and IC-26 is forced to logic 0 because its J input is at logic 0.

Reset is accomplished by taking all C inputs of the flip-flops to a logic 0. These logic levels are supplied by IC-22B. Reset is accomplished by taking all C inputs of the flip-flops to a logic 0. These logic levels are supplied by IC-22B. Counting is started when the J and K inputs of IC-24A are taken to logic 1, and inhibited when these same inputs are returned to a logic 0. Theses logic levels are supplied by the A output of IC-19 or the Q output of IC-15A, through switch S2A.

4-6 SECOND, THIRD, FOURTH, AND FIFTH DECADE COUNTERS

These counters are asynchronous 1-2-4-8 BCD counters that require a single integrated circuit for each decade. The internal operation of these circuits is similar to the first decade pulse counter, so they will not be discussed in detail. The main difference is that no gating is required because when the first counter is not counting, the subsequent counters will not operate. Reset is initiated when the reset lines go to a logic 1 and is accomplished by IC-22D.

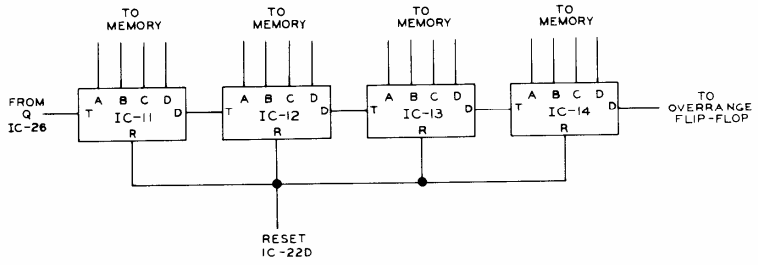


Figure 4-6 — 2ND, 3RD, 4TH, AND 5TH DECADE COUNTERS

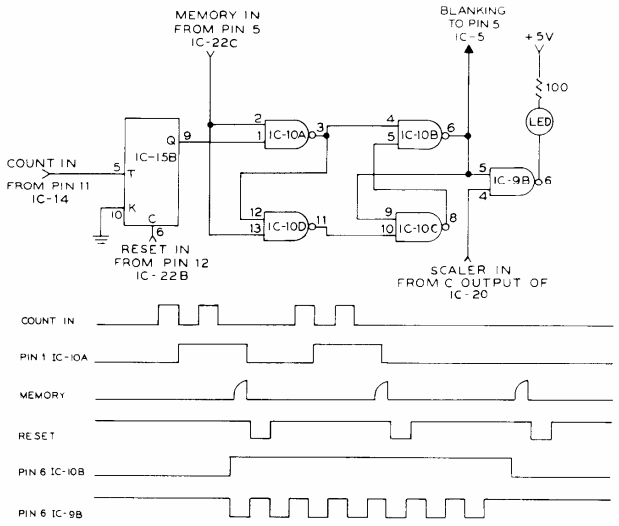
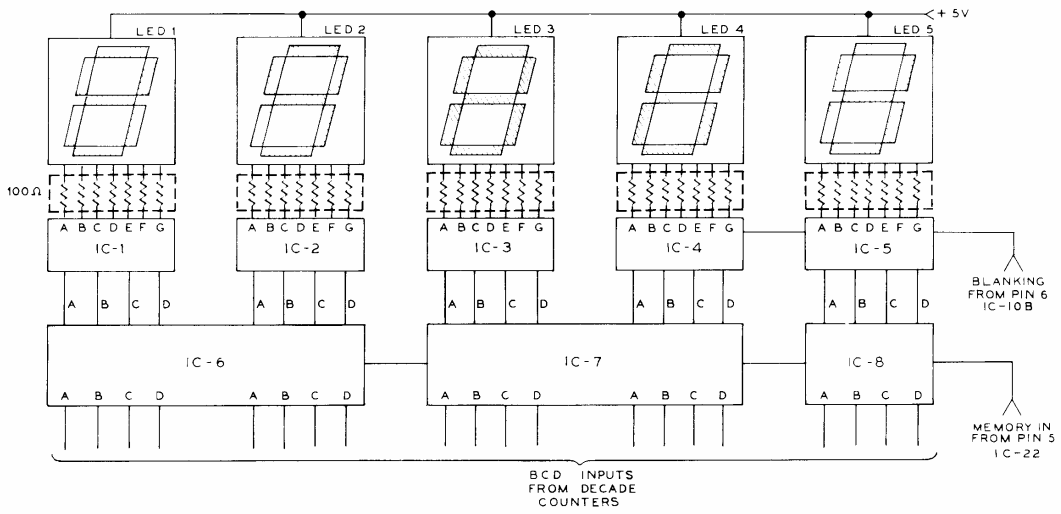


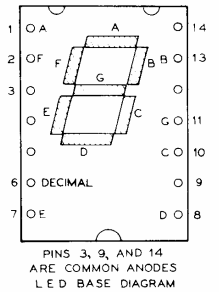
Figure 4-7 — OVERRANGE DETECTOR AND READOUT

4-7 OVERRANGE DETECTION AND READOUT

If the count passes from 99999 to 100000, a pulse at the D output of IC-14 will be produced. This spill-over toggles IC-15 which is a standard J-K flip-flop. The K input of IC-15 is tied to logic 0 which causes the Q output to latch in a logic 1 condition whenever the T input is toggled. The Q output will stay in this condition until a logic 0 is applied to the C (clear) input.

IC-10 is a quad, two-input NAND gate package used as a D-type latch. The logic level at pin 1 of IC-10A will be transferred to pin 6 of IC-10B only when pin 2 of IC-10A and pin 13 of IC-10D are both at logic 1. A logic 0 at these inputs will inhibit transfer. The output of the latch is connected to one input of gate IC-9B. The C output of IC-20 in the scaler is connected to the other input of this gate. Therefore the overrange light will flash whenever there is a logic 1 output from pin 6 of IC-10B, which indicates spill-over from IC-14.





PINS 3, 9, AND 14 ARE COMMON ANODES
LED BASE DIAGRAM

COUNT	BCD INPUT				7-LINE OUTPUT						
	A	B	C	D	A	B	C	D	E	F	G
0	0	0	0	0	0	0	0	0	0	0	1
1	1	0	0	0	1	0	0	1	1	1	1
2	0	1	0	0	0	0	1	0	0	1	0
3	1	1	0	0	0	0	0	0	1	1	0
4	0	0	1	0	1	0	0	1	1	0	0
5	1	0	1	0	0	1	0	0	1	0	0
6	0	1	1	0	1	1	0	0	0	0	0
7	1	1	1	0	0	0	0	1	1	1	1
8	0	0	0	1	0	0	0	0	0	0	0
9	1	0	0	1	0	0	0	1	1	0	0

7-LINE INFORMATION FROM BCD DECODER-DIVIDERS

Figure 4-8 — READOUT AND MEMORY LATCHES

4-8 READOUT AND MEMORY LATCHES

The four-line 1-2-4-8 BCD outputs from the decade counters are connected to the memory latches, IC-6, IC-7, and IC-8. The signals applied to the inputs of these latches are transferred to their outputs when the memory line goes to a logic 1. When the memory line returns to logic 0, the information at the outputs is retained even though the logic level at the inputs may change.

All the information at the outputs of the memory latches is decoded into a seven-line code by the decoder drivers, IC-1 through IC-5, and applied to the seven-segment LED displays. The table in Figure 4-8 shows how this input signal is decoded. A logic 0 is required by each segment for turn on. If a code other than BCD or a BCD count which exceeds 9 is received by the decoder-driver, the display will not register valid information. If this should happen, the next reset and memory pulse will remove the illegal codes and subsequent displays will be valid.

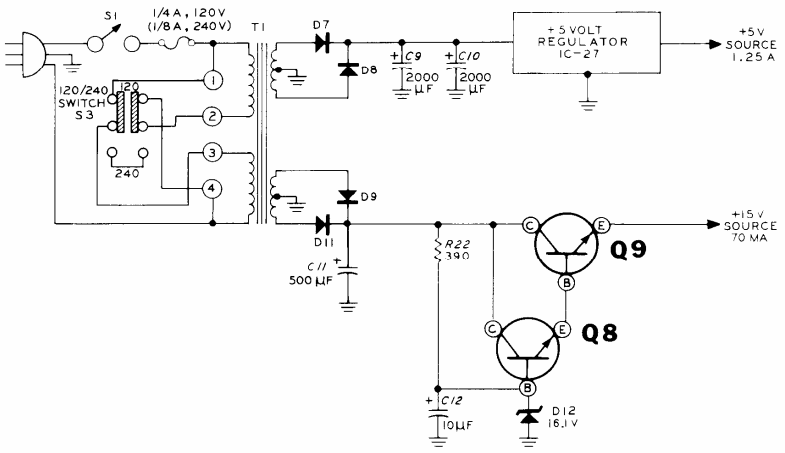


Figure 4-9 — POWER SUPPLY SCHEMATIC

4-9 POWER SUPPLY

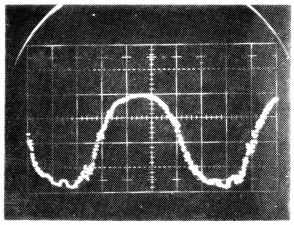
Two regulated dc power supplies operate from secondary windings of the power transformer. One provides +5 volts at 1.25 amperes, and the other supplies +15 volts at 70 milliamperes. Each supply has full-wave rectification, capacitive filters, and series regulator, as shown in Figure 4-9. Since the +5 volt supply uses an integrated regulator, only the +15 volt supply will be discussed.

The rectified voltage from diodes D9 and D11, filtered by capacitor C11, is applied to the regulator. Transistors Q8 and Q9 are connected as a Darlington-pair pass transistor. Zener diode D12 provides a 16.1 volt reference to the base of Q8. The output of this regulator is the reference source voltage minus the bass-emitter drop across the Darlington pair. With the zener diode biased in its zener region by resistor R22, regulation is maintained over the normal load range of the regulator.

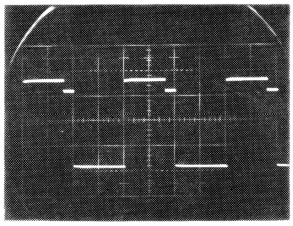
4-10 BLANKING

All the logic required for blanking the insignificant zeros is included as part of the decoder-driver integrated circuits (IC-4 and IC-5) which operate as follows: Overrange information from IC-10 is routed to the ripple blanking input (RBI), pin 5 of IC-5. A logic 1 at this point (overrange light flashing) unblanks IC-5 and IC-4 for any BCD input condition. If, however, pin 5 of IC-5 is logic 0 (overrange light off), IC-5 will be blanked for a BCD code of 0 and unblanked for any other code. The ripple blanking output (RBO), pin 4 of IC-5, will be at a logic 0 if IC-5 is blanked and at a logic 1 if it is unblanked. This terminal is connected to the RBI terminal of IC-4 which operates in the same manner as IC-5. Thus, LED-4 will be blanked if LED-5 is blanked, LED-6 is off and IC-4 has logic 0 at all of its BCD terminals; otherwise it will be unblanked. LED-5 will be blanked if LED-6 is off and IC-5 has logic 0 at all of its BCD terminals; otherwise it wil be unblanked.

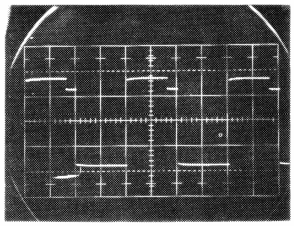
NOTE: All waveforms taken with Tektronix 547 with 1A4 plug-in, except waveform #1



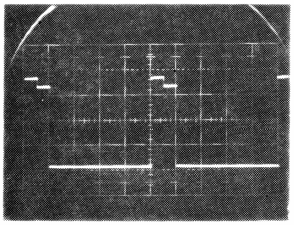
#1
Pin 1 of IC-24A (output from Q7)
Counter input, 80 MHz at 250 mV
Scope setting, 2 ns/cm and 1 V/cm
(Use Tektronix 1S1 plug-in and
P6035 probe.)



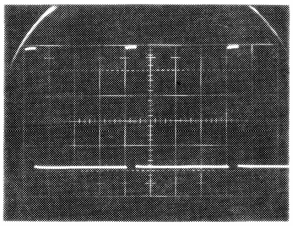
#2
Pin 4 of IC-23, MHz time base
Scope settings, 0.5 ms/cm and 1 V/cm



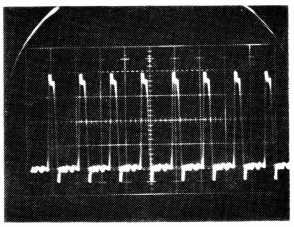
#3
Pin 12 of IC-21
Scope settings, 5.0 ms/cm and 1 V/cm



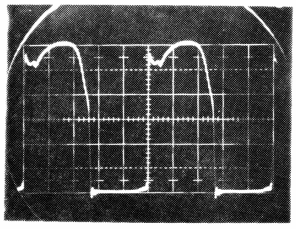
#4
Pin 13 of IC-22, MHz time base
Scope settings, 0.2 ms/cm and 1 V/cm



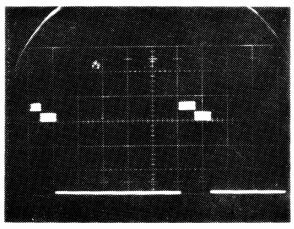
#5
Pin 2 of IC-11, MHz time base
Scope settings, 0.5 ms/cm and 1 V/cm



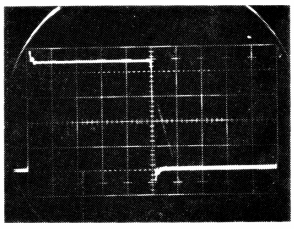
#6
Pin 8 of IC-26, 8 MHz signal
80 MHz input
Scope settings, 0.1 us/cm and 1 V/cm



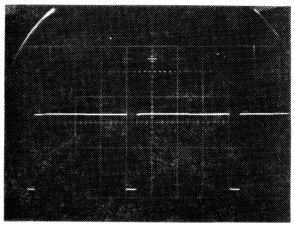
#7
Test point 1, 1 MHz oscillator
Scope settings, 0.2 us/cm and .5 V/cm



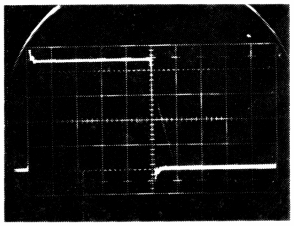
#8
Pin 11 of IC-24, 800 Hz signal
80 MHz input, kHz time base
Scope settings, 0.2 mx/cm and 1 V/cm



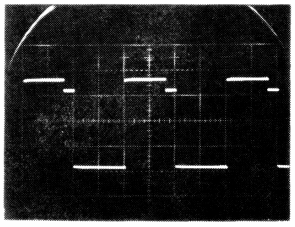
#9
Emitter of Q7
100 kHz input
Scope settings, 1 us/cm and 1 V/cm



#10
Pin 12 of IC-22, MHz time base
Scope settings, 0.2 us/cm and 1 V/cm



#11
Pin 12 of IC-7
Scope settings. 10 us/cm and 1 V/cm



#12
Pins 2 and 3 of IC-24A, Gate Pulse
Scope settings, 0.5 ms/cm and 1 V/cm

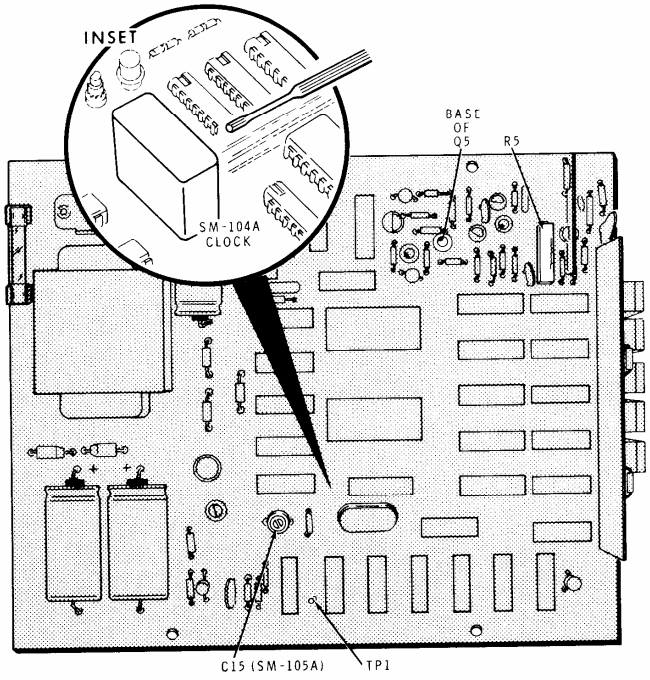


Figure 6-1 — LOCATION OF TEST POINT AND ADJUSTMENTS

SECTION 6

CALIBRATION

Calibration of this instrument should not be attempted unless you are experienced and qualified in the use of precision laboratory equipment. The equipment required for calibration should have specifications that are at least ten-fold better than the instrument being calibrated.

The following Input Amplifier Adjustments can be made in either the SM-104A or SM-105A Counter. Separate Clock Calibration instructions are presented for each of the two Counters.

INPUT AMPLIFIER ADJUSTMENTS

Figure 6-1 shows the location of the adjustment and test point used in the following steps.

1. Allow the Counter to warm up for approximately 1 hour, then short the input cable leads together and adjust control R5 for a reading of +6.5 volts at the base of transistor Q5.

2. With the Time Base switch in the MHz position, connect an 80 MHz, 500 millivolt rms, signal to the input and readjust R5 for the most stable display on the LED readout.

3. Decrease the level of the input signal until the readout becomes unstable and again readjust R5 for a stable readout.

4. Repeat Step 3 until best input sensitivity is obtained.

CLOCK CALIBRATION

The following adjustments should not be attempted unless you have extremely accurate test equipment. We strongly recommend that you return the Counter to the Heath Company if you are certain that calibration is necessary. For Factory Repair Service, refer to the Service Information on the inside rear cover of this Manual.

SM-105A Calibration

Figure 6-1 shows the location of the adjustment used in the following step.

1. With the Time Base switch in the kHz position, connect a 1 MHz, signal, accurate to $\pm$0.1 Hz, to the input of the Counter. Then adjust capacitor C15 for a readout of 1 MHz $\pm$2 Hz on the LED display. This completes the SM-105A calibration.

SM-104A Calibration

Figure 6-1 shows the location of the test point and adjustment used in the following steps.

NOTE: A frequency measurement or comparison instrument with accuracy of at least one part in 10^8 must be used to calibrate the clock.

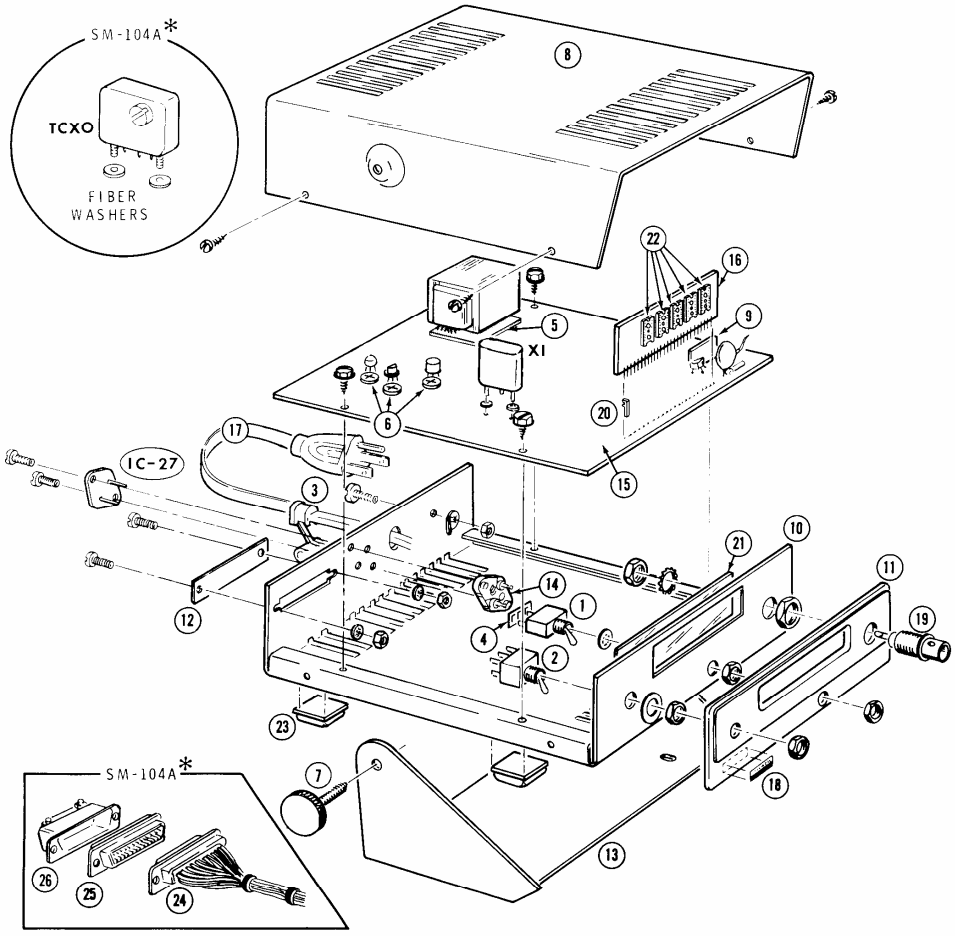
1. Connect the frequency measurement instrument (and comparison instrument if used) to TP-1 on the circuit board. This is the 1 MHz clock output.

2. Remove the screw from the side of the oscillator assembly and insert a nonmetallic alignment tool. Adjust the oscillator until the output frequency is 1 MHz, $\pm$0.1 Hz.

Note that the oscillator adjustment can vary the crystal frequency only a few parts per million. If the measured or compared frequency deviates more than that amount, suspect your test equipment before you suspect the oscillator assembly.

This completes the SM-104A calibration.

CHASSIS AND CABINET PARTS PICTORIAL



SECTION 7

APPENDIX

The same electronic component designations are used on the X-Ray Views and Schematic Diagram as in the Replacement Parts List. This simplifies the identification of parts for ordering, or for circuit tracing.

REPLACEMENT PARTS LIST

Write to the Heath Company for price information on any of the following prices.

CHASSIS AND CABINET COMPONENTS

KEY No.	PART No.	DESCRIPTION
SWITCHES		
1	61-16	SPDT switch with hardware
2	61-17	DPDT switch with hardware
INSULATORS		
3	75-71	Line cord strain relief
4	75-149	Switch insulator
5	73-84	Vinyl foam gasket
6	75-158	Transistor insulator
HARDWARE METAL PARTS		
7	250-527	Thumbscrew
8	90-519-1	Cabinet shell
9	215-55	Heat sink
10	200-632-1	Chassis
11	203-864	Decorative front panel
12	205-858-1	Rear panel hole cover plate**
13	204-1195	Gimbal bracket

KEY No.	PART No.	DESCRIPTION
MISCELLANEOUS		
14	434-117	Transistor socket
15	85-1147	Main circuit board
16	85-1146	Readout circuit board
17	89-23	Line cord
18	390-928	Heath/Schlumberger label
19	432-91	BNC connector with hardware
20	432-734	Circuit board connector
21	446-85-1	Plastic window
22	434-217	I.C. socket
23	261-34	Plastic foot
24	134-284	BCD Wiring harness*
25	432-718	Rear panel BCD connector*
26	432-719	Connector shell*

*Indicates parts used in SM-104A only.
**Indicates parts used in SM-105A only.

MAIN CIRCUIT BOARD COMPONENTS

COMPONENT DESIGNATION	PART No.	DESCRIPTION
RESISTORS AND CONTROLS		
(All resistors 1/4-watt, 10% unless otherwise noted.)		
R1	1-19-12	1 MΩ
R2	9-49	680 Ω 2-1/4-watt, 5%
R3	1-62-12	220 Ω 5%
R4	1-61-12	180 Ω 5%
R5	10-345	1/2-watt, 500 Ω control
R6	1-61-12	180 Ω 5%
R7	1-54-12	68 Ω
R8	1-67-12	680 Ω 5%
R9	1-60-12	100 Ω 5%
R10	NOT USED	
R11	1-67-12	680 Ω 5%
R12	1-42-12	22 Ω
R13	1-64-12	5%, 390 Ω
R14	1-24-12	820 Ω
R15	1-62-12	220 Ω 5%
R16	1-54-12	68 Ω
R17	1-2-12	1000 Ω
R18	1-2-12	1000 Ω
R19	1-64-12	390 Ω 5%
R20	1-60-12	100 Ω 5%
R21	1-2-12	1000 Ω
R22	1-64-12	390 Ω
R23, R24, R25, R26, R27	NOTE: R23 THROUGH R27 RESISTOR MODULES Part#9-43, 100 Ω if LED is 412-69 Part#9-53, 180 Ω if LED is 412-77	
R28	1-67-12	680 Ω **
R29	1-67-12	680 Ω **
R30	NOT USED	
R31	1-37-12	150 Ω **
CAPACITORS		
C1	21-82	.02 μF
C2	21-3	10 pF
C3	21-27	.005 μF
C4	20-76	68 pF
C5	21-27	.005 μF
C6	25-220	10 μF
C7	25-220	10 μF
C8	20-107	680 μF
C9	25-230	2000 μF
C10	25-230	2000 μF
C11	25-199	500 μF
C12	25-220	10 μF
C13	21-27	.005 μF **
C14	21-78	5 pF **
C15	31-58	1.7-10 pF ceramic trimmer**
C16	25-220	10 μF
DIODES		
D1	56-86	FD 777 diode
D2	56-86	FD 777 diode
D3	56-86	FD 777 diode
D4	56-59	1N750 A 4.7 V zener
D5,	56-61	Stabistor
D6	NOT USED	
D7	57-42	3A1 diode
D8	57-42	3A1 diode
D9	57-65	1N4002 diode
D10	NOT USED	
D11	57-65	1N4002 diode
D12	56-36	VR 16.1G zener
TRANSISTORS		
Q1	417-288	Selected 2N4416
Q2	417-260	2N4258A
Q3	417-125	2N3563
Q4	417-134	MPS6520
Q5	417-260	2N4258A
Q6	417-260	2N4258A
Q7	417-125	2N3563
Q8	417-118	2N3393
Q9	417-220	SS9327
INTEGRATED CIRCUITS		
IC-1	443-36	SN7447N
IC-2	443-36	SN7447N
IC-3	443-36	SN7447N
IC-4	443-36	SN7447N
IC-5	443-36	SN7447N
IC-6	443-37	SN74100N
IC-7	443-37	SN74100N
IC-8	443-13	SN7475N
IC-9	443-1	SN7400N
IC-10	443-1	SN7400N
IC-11	443-7	SN7490N
IC-12	443-7	SN7490N
IC-13	443-7	SN7490N
IC-14	443-7	SN7490N
IC-15	443-5	SN7473N
IC-16	443-7	SN7490N
IC-17	443-7	SN7490N
IC-18	443-7	SN7490N
IC-19	443-7	SN7490N
IC-20	443-7	SN7490N

COMPONENT DESIGNATION	PART No.	DESCRIPTION
IC-21	443-7	SN7490N
IC-22	442-19	SN75450N
IC-23	443-1	SN7400N
IC-24	443-42	SN74S112N
IC-25	443-43	SN74N102N
IC-26	443-43	SN74N102N
IC-27	442-30	μA-309-K

MISCELLANEOUS

S3	60-68	DPDT slide switch
T1	54-270	Power transformer
X1	404-424	1 MHz crystal **
TCXO	150-27	Temperature compensated crystal oscillator*
Fuse	421-33	1/4 ampere fuse
F.C.	260-65	Fuse clip

READOUT BOARD COMPONENTS

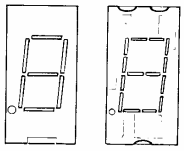
(See Figure 7-1)

COMPONENT DESIGNATION	PART No.	DESCRIPTION
R1	1-23-12	390 Ω 1/4-watt resistor
	1-1-12	100 Ω 1/4-watt resistor
R2	1-1-12	100 Ω 1/4-watt resistor
LED-1	412-69	Seven segment LED
	412-77	Seven segment LED
LED-2	412-69	Seven segment LED
	412-77	Seven segment LED
LED-3	412-69	Seven segment LED
	412-77	Seven segment LED
LED-4	412-69	Seven segment LED
	417-77	Seven segment LED
LED-5	412-69	Seven segment LED
	412-77	Seven segment LED
LED-6	412-70	Single LED

* Used in SM-104A only.

** Used in SM-105A, SM-105AS, and SM-105AW only.

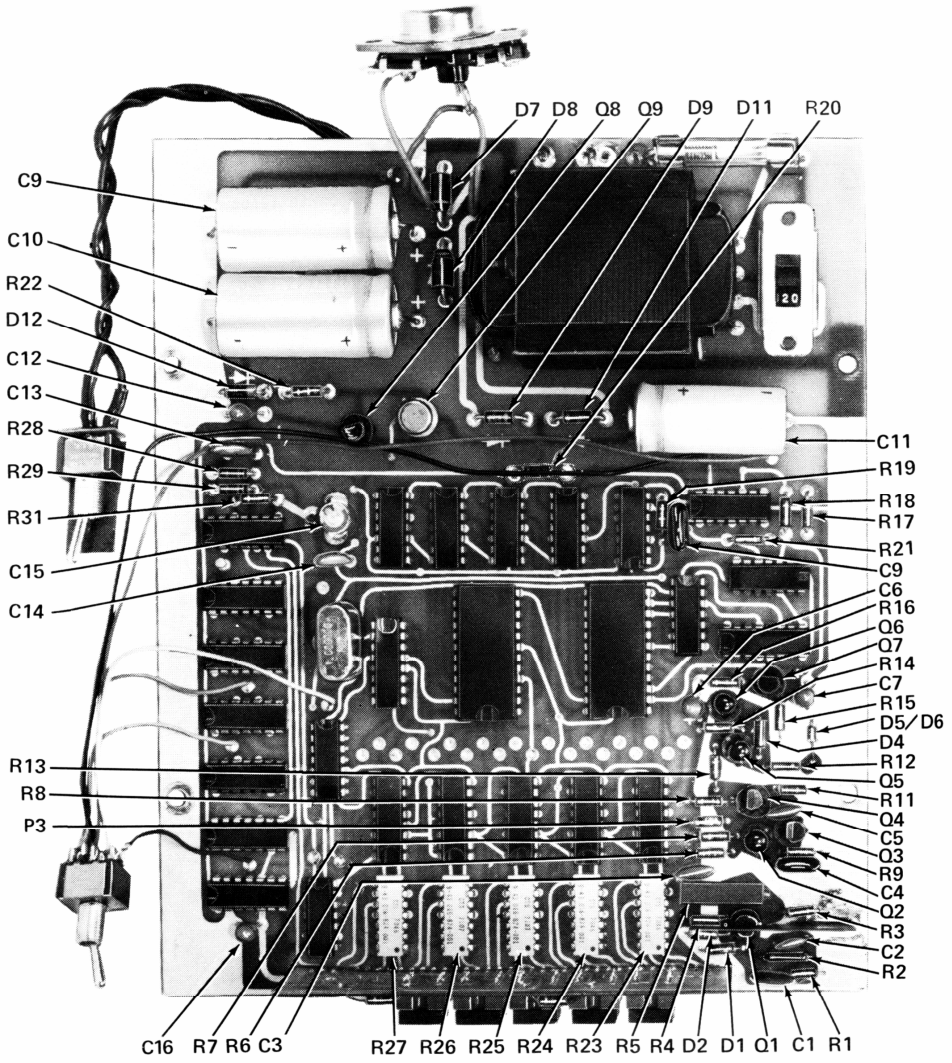
Figure 7-1



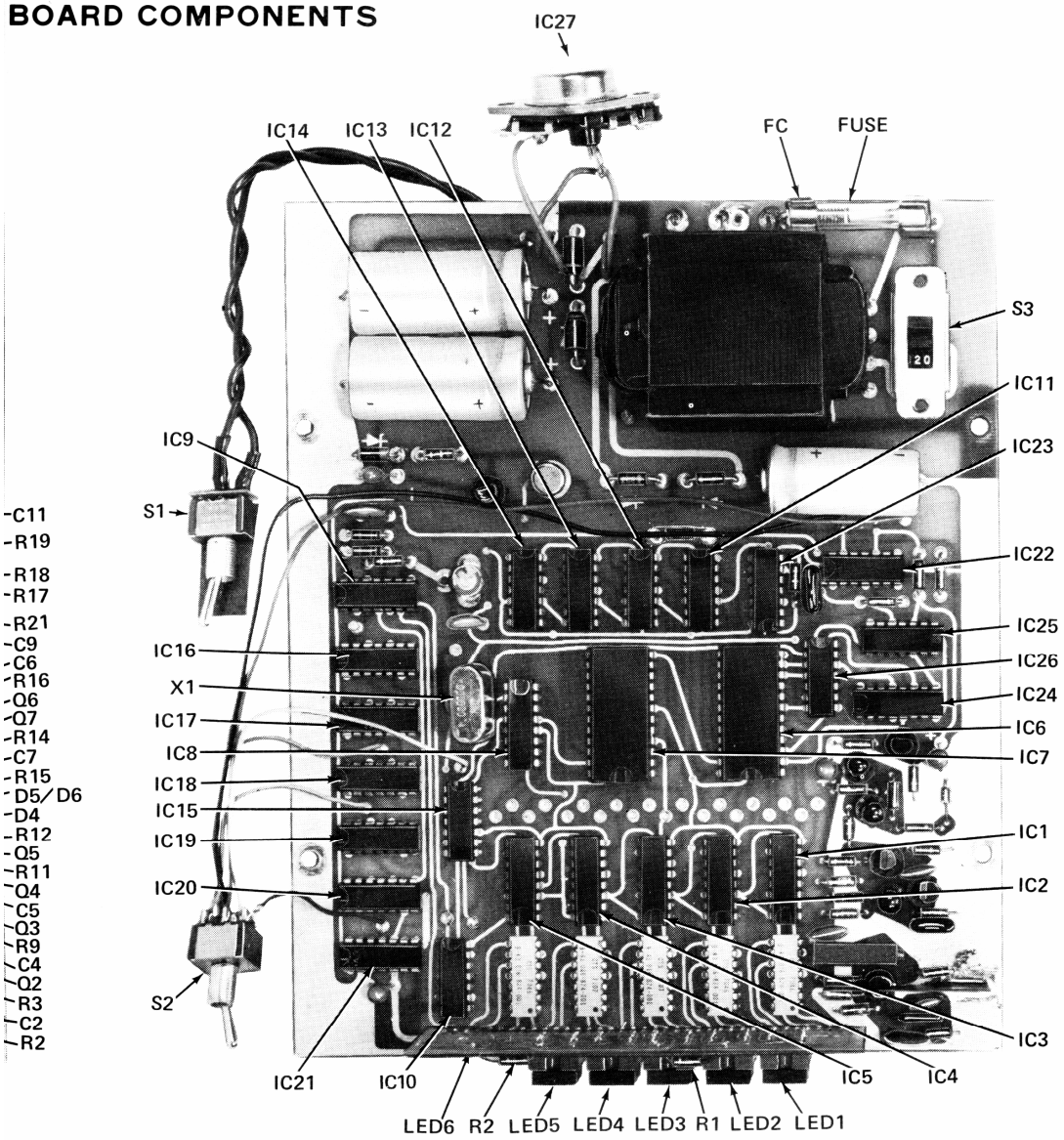
RESISTORS R1 AND R2 ARE MOUNTED ON THE READOUT CIRCUIT BOARD.
R1 IS 390Ω WHEN LED-3 IS 412-69
R1 IS 100Ω WHEN LED-3 IS 412-77

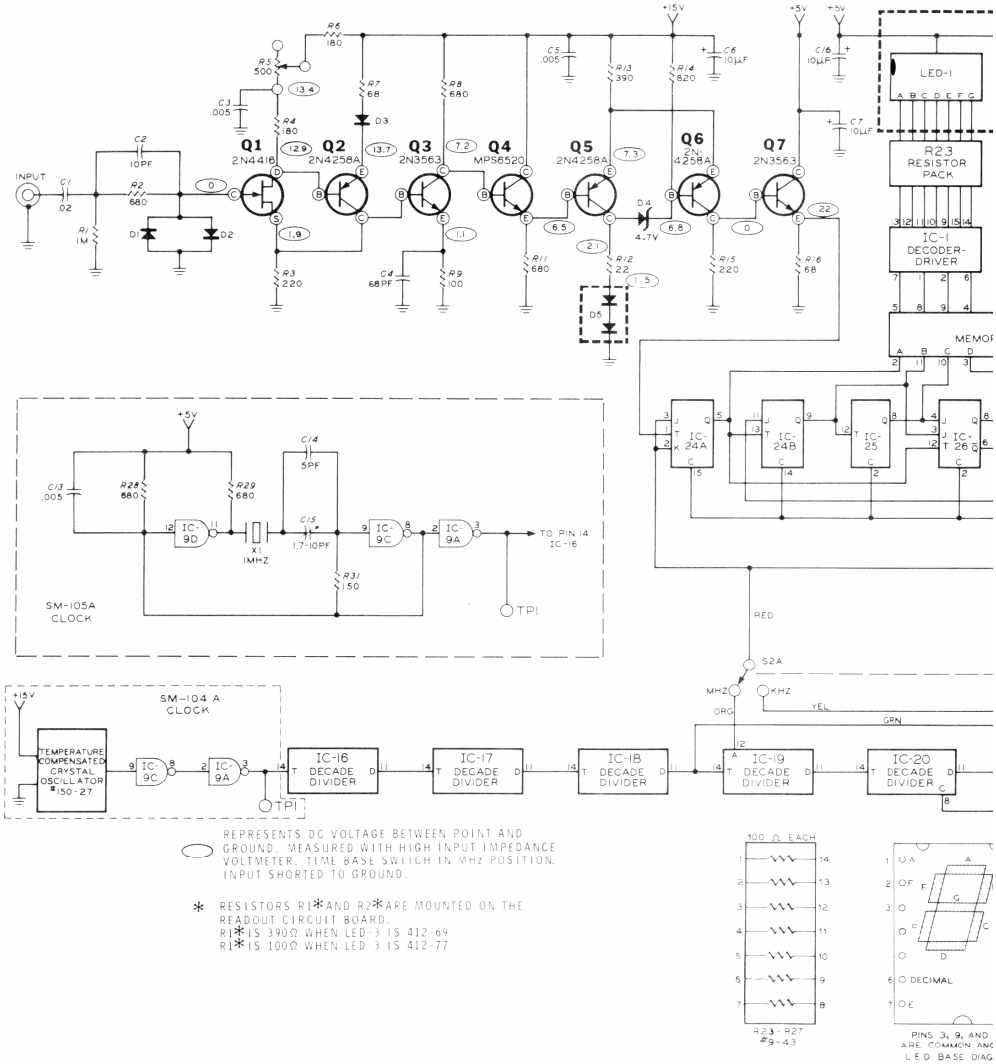
LED IDENTIFICATION

CIRCUIT BOARI



BOARD COMPONENTS

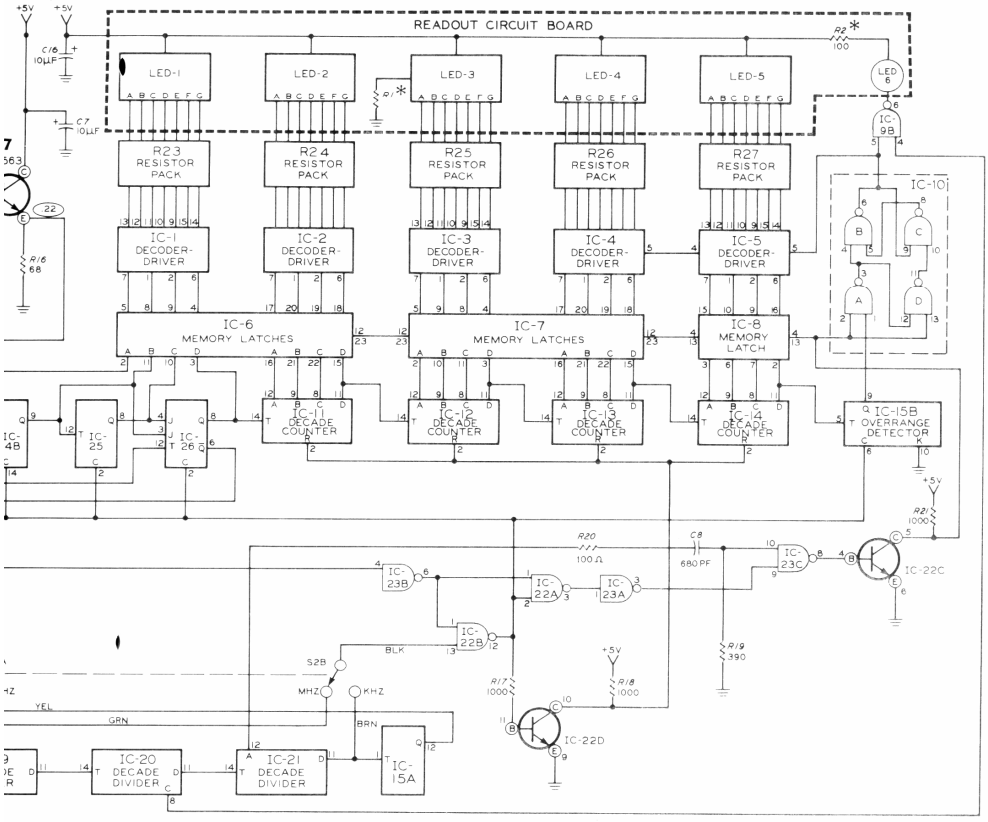




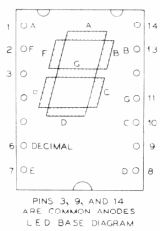
REPRESENTS DC VOLTAGE BETWEEN POINT AND GROUND. MEASURED WITH HIGH INPUT IMPEDANCE VOLTMETER. TIME BASE SWITCH IN MHZ POSITION. INPUT SHORTED TO GROUND.

* RESISTORS R1* AND R2* ARE MOUNTED ON THE READOUT CIRCUIT BOARD.
R1* IS 390Ω WHEN LED-3 IS 412-69
R1* IS 100Ω WHEN LED-3 IS 412-77

SCHEMATIC OF THE HEATH SOLID-STATE COUNTER MODEL SM-105A



SCHEMATIC OF THE
HEATH
SOLID-STATE COUNTER
MODEL SM-105A



PINS 3, 9, AND 14
ARE COMMON ANODES
LED BASE DIAGRAM